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Integrated Circuits for XRD Imaging

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3.1 Introduction

As discussed in Chapter 2, XRD application requires specialized circuit electronics. Early developments in this field were using discrete electronics, but over the past decade, the signal processing has been done mostly with Integrated Circuits (ICs), also called Application-Specific Integrated Circuits (ASICs), that are either directly or through the joining interposer attached to the semiconductor sensors. Modern integrated circuit technology makes it economically feasible for each pixel to have its own low-noise electronics, creating what are known as “hybrid pixel detector readout ASICs.” The purpose of this chapter is to review some fundamentals of this readout IC electronics and present some examples of its implementation by various industrial vendors and research organizations worldwide.

Radiation detectors detect and convert radiation into electric signals. The amount of charge, \( Q \), generated by an ionizing event is proportional to energy deposited in the detector. Almost all X-ray detection applications require either discriminating or measuring \( Q \) and, in some cases, its time of arrival. The detector has at least two electrodes but frequently has a larger number, especially on one of its sides (e.g., pixelated-, strip-, co-planar, or Frish grid-detectors, as discussed in Chapter 2). An electric field is generated in the detector, most often by applying a voltage between the pixelated (or segmented) electrodes on one side and a common electrode on the opposite side. Under this electric field, the ionized charge, \( Q \), moves toward one or more electrodes inducing a charge flow in each.

Depending upon the type of detector and the particular application, the charge can be read out event by event or it can be integrated from several events in the capacitance of the electrode and read out at a later time. In most cases discussed in this book, photons arrive randomly in time domain. Invariably, reading out the signals from radiation detectors requires highly specialized electronics, usually referred to as “front-end” electronics. This electronics usually entails stringent requirements in terms of the signal-to-noise ratio, dynamic range, linearity, and stability.

A typical front-end channel is composed of three fundamental blocks: the low-noise amplifier, the filter (usually referred to as the “shaper”), and the peak detector. The low-noise amplifier reduces the relative noise contribution from the next blocks, i.e., the shaper and peak detector, to negligible levels. The shaper is required to optimize the signal-to-noise ratio, while the peak detector (PD) provides discrimination, measurement, and storage depending on the application (e.g., waveform discrimination and counting, waveform peak and/or timing, and periodic sampling).

Application of semiconductor detectors requires use of dedicated detector electronics. The signal generated by X-ray sensors needs to be amplified, filtered, and possibly stored by analog circuitry for subsequent conversion to digital signal domain for further processing. Analog signal processing
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requires use of dedicated discrete electronics or application-specific integrated circuit (ASIC). Digital processing typically requires use of FPGA to control analog front end.

3.2  Readout ICs Fundamentals

3.2.1  IC Technology

Semiconductor-pixelated detectors need to have a high level of segmented multi-channel readout. Several decades ago, the only way to achieve this was via massive fan-out schemes to route signals to discrete low-density electronics. At the present time, CMOS technology is used to build very dense low-power electronics with many channels which can be bonded directly or indirectly (through a common carrier PCB) to the detector.

There are different requirements for the CMOS technology used for the analog front-end signal processing, as opposed to that of the digital signal processing. For the analog part of the electronics, there is a requirement for a robust technology that has low electronic noise and high-dynamic range that typically requires high power supply voltages. Digital signal processing in turn requires very high speed and high density that is more compatible with the more modern low-voltage supply, deep submicron processes.

There seems to be a technology optimum at around 0.35 μm to 0.18 μm minimum feature size for the analog requirements. The large feature size limits the complexity of circuitry that can be integrated in a pixel but even at 0.35 μm it is possible to place a million transistors on a reasonable size silicon die. In comparison, digital signal processing can benefit from the rapid development of deep submicron processes. Some selected research developments now take place using 90 nm or 65 nm process nodes. These technologies are well suited to high-speed ADC architectures and to very fast data manipulation for data sparcification and compression. The deep submicron technologies have their own limitations in terms of analog performance, noise, and cost.

A block diagram of the typical charge detection electronics for each pixel or channel is shown in Figure 3.1 [1–3].

The charge generated by the semiconductor sensor $Q_0$ (in this example, CZT sensor is being shown) enters a Charge-Sensitive Amplifier (CSA), which converts the charge to a voltage using the feedback capacitor $C_f$:

$$V_{CSA} = \frac{Q_0}{C_f}$$

As an example, let us assume $C_f$ value of 10 fF. Since a 59.5 eV photon produces 1.9 fC of charge, this corresponds to a step change of 190 mV at the CSA output, a reasonably large value to be detected.
The transient $V_{\text{CSA}}$ step then enters a bandpass filter to improve the signal-to-noise ratio. Since this bandpass filter changes the shape of the $V_{\text{CSA}}$ response, it is also called a pulse shaper. The peak output of the shaper is compared to a programmable threshold to determine if a valid pixel event has occurred; this comparison is done to remove false events due to noise. Finally, a valid pixel event is digitalized using an ADC for further downstream processing. An example of signal processing is shown in Figure 3.2.

Front-end ASIC electronics is an important part of the entire signal processing chain. However, in order to facilitate the integration of semiconductor sensors in end-customer XRD systems, a further signal processing is required, frequently referred to as X-ray detection module. A block diagram of such a module is shown in Figure 3.3. Ethernet PHY block represents I/O...
transceiver as an example, as other I/O technologies like Camera Link, Fibre Channel, or Rapid I/O Phy can be used as well depending on the requirement on the connecting external PC host environment.

3.2.2 IC Design Process

IC design process contains the following phases to take place until device tape-out (TO) to the selected foundry as schematically illustrated in Figure 3.4.

- Feasibility Phase – During the feasibility phase, the design team is expected to perform architectural development for the proposed readout IC solution. All relevant process and fabrication arrangements have to be finalized at that stage by the design team. Computer Aided Design (CAD) technology files have to be installed in the IC design flow at that time. The feasibility phase ends with a Design Start review where the design team discusses with the proposed solution and all outstanding issues, if any, are clarified.

- Design/Simulation Phase – During the simulation phase, the design team is expected to perform SPICE simulation results for the detailed circuit implementation of the IC.

- The design phase ends with a Design Simulation review where the design team presents detailed circuit simulation results. It is expected that the design team will provide a written engineering report that contains circuit simulation results before proceeding to the next stage as required by concurrent design and documentation good practices.
• Layout Phase – During the layout phase, the design team is expected to perform IC layout in a given manufacturing process. All layout implementation issues have to be finalized by the design team at that stage. Any post-layout simulation results that would indicate a necessity to revise circuit schematics have to be reported immediately to
the designated representative. The layout phase ends with a Design Layout review. It is expected that the design team will provide an updated written engineering report that contains post-layout circuit simulation results before proceeding to the next stage (concurrent design and documentation).

- Verification Phase – During verification phase, the design team is expected to perform exhaustive verification of the completed design before submitting the design for tape-out (TO). For example, device mismatch, power supply noise, substrate crosstalk, I/O ground bounce, etc. have to be taken into account. ASIC verification for reliability requirements: interconnect/via electromigration, ESD, and latch-up is expected as well. It is essential that the verification be performed in conjunction with the CZT detector model, package, and PCB parasitic elements. During that phase, the design team completes a test plan for the prototype evaluation phase to be followed. It is expected that the entire engineering documentation is complete before proceeding to the tape-out (TO). The verification phase ends with Design End review.

3.2.3 Photon Counting vs. Spectroscopy

There are two ways of signal processing for XRD with energy-sensitive semiconductor detectors: photon counting and spectroscopy. While precise difference between the two might be hard to establish as all analog signals eventually become digital at some point in the readout system, we would like to suggest the following practical definition. Photon counting relies on energy binning using comparators inside the readout IC chip. Spectroscopy in turn preserves the analog nature of the signal representing photon energy with an A/D converter after the readout IC signal processing has been accomplished.

As a result of this architectural change, photon counting systems can achieve very high count rate while sacrificing energy resolution (ER), while spectroscopic system can have very good noise properties but face limitations with a maximum count rate. To achieve specific design objectives, either count rate of the spectroscopic system or energy resolution of the photon-counting systems is maximized. Schematic comparison between two types of signal processing is shown in Figure 3.5.

3.2.4 Photon Counting ICs

One of the major advantages of photon-counting detectors is electronics noise rejection. Well-designed photon-counting detectors allow for ASIC electronics threshold high enough to reject noise pulses while still counting useful signals. Therefore, quantum limited operation of the photon-counting detector can be achieved as image noise is determined only by statistical
variations of X-ray photons. On the other hand, energy-integrating detectors suffer from electronics noise which is mixed with useful photon signals and separating it from statistical noise is not possible. Electronics noise rejection is important because its magnitude for currently used digital X-ray detectors is not negligible.

After converting the CZT-generated charge to voltage by the CSA and subsequent filtering by the shaping amplifier, the signal is ready for digitization. Typically, the signal is compared against user selected threshold voltage (discriminator box in Figure 3.6) to produce 1-bit trigger signal indicating detection of the pulse. In parallel, the value of the shaped signal is sent to an ADC converter (or Time over Threshold, or ToT, processor) with n-bit accuracy. The conversion resolution $n$ is typically between 8 and 16 bits depending on the system accuracy, noise levels, and degree of signal precision achieved. One important consideration in the practical system is CSA reset. As the feedback capacitor $C_f$ is charged by the input signal, there must be some means of discharging this capacitor in order for the CSA to be ready for the next signal. This circuitry is schematically shown as the reset block in Figure 3.6.

There are two possible implementations for the reset block: digital and analog. The digital one involves using a switch that will discharge the feedback capacitor quickly. Unfortunately, this process typically creates too much disturbance for the sensitive CSA. The analog solution involves using
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a resistor (or MOSFET operating in the triode region) and provides continuous discharging during the entire process. The discharge cannot be too slow (in which case, the capacitor will not be fully discharged before the next event) or too fast (as that will affect signal formation). While the CZT readout scheme shown in Figure 3.6 is a typical implementation, it is possible to directly sample the signals without producing any trigger signal to obtain timing and amplitude information.

On a final note, while the principle of CSA signal amplification, pulse shaping, and ADC conversions outlined above are fairly simple, practical implementations can be very challenging due to very small input signals involved (below 1 mV). One has to pay particular attention to system noise, power supply decoupling, ESD protection, EMI radiation, and op-amp stability issues.

A typical photon counting ASIC implementation contains hundreds of channels frequently implemented with multiple energy bins. A typical 128-channel ASIC architecture is shown in Figure 3.7.

### 3.2.5 Spectroscopic ICs

XRD detectors typically operate in a single photon detection mode where an electric charge generated by one photon needs to be collected by the readout electronics. As the amount of generated charge is small (few femto Columbs, fCs), very sensitive analog circuitry is required to amplify that charge. In spectroscopic applications, the amount of charge, which directly corresponds to the photon energy, needs to be precisely determined. In photon-counting applications, only binary (or multi-binary) decision is required but the count rate might be very high creating its related challenges. The purpose of this section is to explain some of the design considerations that are important when building XRD readout electronics systems.
3.2.5.1 Analog Front-End

Analog signal processing can be divided into the following steps:

- Amplification – The input charge signal is amplified and converted to a voltage signal using a CSA. The main characteristic of the amplification stage is Equivalent Noise Charge (ENC) which is required to be as low as possible in order not to degrade intrinsic detector energy resolution. Another important consideration for the CSA operation is a dark current compensation mechanism. A solution that accommodates continuous compensation for dark currents up to several nAs while maintaining low ENC is desired.

- Signal shaping – The time response of the system is tailored to optimize the measurement of signal magnitude or time and the rate of signal detection. The output of the signal chain is a pulse whose area is proportional to the original signal charge, i.e. the energy deposited in the detector. The pulse shaper transforms a narrow detector current pulse to broader pulse (to reduce electronic noise), with a gradually rounded maximum at the peaking time to facilitate measurement of the amplitude. A solution that provides effective signal shaping while maximizing the channel count rate needs to be applied.

- Pulse detection – The input pulse, broadened by the shaping process, needs to be detected against a set-up threshold value. The
threshold level is a critical parameter that determines whether the event is recognized as a true event or false reading caused by noise. As a result, the threshold value is typically adjustable both globally and at the pixel level. The peak detection value determines energy-level information. A solution that prevents temperature drift of the PD needs to be used.

- Channel multiplexing – In case of ASIC spectroscopy, all parallel channels of the channel readout ASIC need to have their signals multiplexed at the output before being sent out to an external ADC. The key requirement to channel multiplexing and signal shaping is a maximum channel count rate determined by the given application.

### 3.2.5.2 Charge-Sensitive Amplifier

For single photon detection, very sensitive analog circuitry is required to amplify the charge generated by the X-ray sensor. The current signal induced in the sensing electrode can be integrated in the pixel capacitance and read out with a high input impedance stage, which amplifies the resulting voltage at the pixel node or it can be read out directly with a low input impedance stage, which amplifies the charge $Q$ and keeps the pixel node at a virtual ground, such as a charge amplifier. The latter is the preferred choice since, among its other advantages, it stabilizes the sensing electrode by keeping its voltage constant during the measurement and/or the read out.

In both cases, low-noise amplification is required to reduce the noise contribution from the processing electronics (such as the shaper, peak detector, and ADC) to negligible amount; good design practice dictates maximizing this amplification while avoiding overload of subsequent stages. This low-noise amplification would also provide either a charge-to-voltage conversion (e.g., source follower, charge amplifier) or a direct charge-to-charge (or current-to-current) amplification (e.g., charge amplifier with compensation, current amplifier). Depending upon this choice, the shaper would be designed to accept a voltage or a current, respectively, as its input signal.

In a properly designed low-noise amplifier, the noise is dominated by processes in the input transistor. Assuming that CMOS technology is employed in the design, the input transistor is referred to as the “input MOSFET” although the design techniques can easily be extended to other types of transistors, such as the JFET, the bipolar transistor, or the hetero-junction transistor. The design phase, which consists of sizing the input MOSFET for maximum resolution, is called “input MOSFET optimization” and has been studied extensively in the literature.

### 3.2.5.3 Equivalent Noise Charge

Equivalent noise charge (ENC) expresses an amount of noise that appears at the chip input in the absence of useful input signal and is a key chip
parameter that affects the energy resolution of the system. Following the standard approach, the total ENC can be divided into three independent components: the white thermal noise associated with the input transistor of the CSA (ENC$_{th}$), the flicker noise associated with the input transistor of the CSA (ENC$_{1/f}$), and the noise associated with the detector dark leakage current (ENC$_{dark}$). Noise arising in other components connected to the ASIC input node such as the bias resistor is generally made negligible in a properly designed system. For a first-order shaper, the ENC components can be approximately expressed as:

$$
ENC_{th}^2 = \left( \frac{8}{3} \right) \frac{kT}{T_{peak} \times g_m} \times C_{tot}^2
$$

$$
ENC_{1/f}^2 = \left( \frac{K_f}{2} \right) \times WL \times \frac{C_{tot}^2}{C_{inp}^2}
$$

$$
ENC_{dark}^2 = 2q \times I_{dark} \times T_{peak}
$$

$$
ENC = \left( ENC_{th}^2 + ENC_{1/f}^2 + ENC_{dark}^2 \right)^{1/2}
$$

where $g_m$ is the transconductance of the CSA input transistor, $C_{tot}$ is the total capacitance at the input of the CSA, $T_{peak}$ is the shaper peaking time, $K_f$ is the CSA input transistor flicker noise constant, $W$ and $L$ are input transistors width and length, and $I_{dark}$ is the detector leakage current. Note that $C_{tot}$ is the sum of the detector capacitance $C_{det}$, the gate-source and gate-drain capacitances of the input transistor $C_{inp}$, and any other feedback or parasitic capacitance at the CSA input originating from the chip package, ESD diodes, and PCB traces. Based on experience with ASIC design and radiation detection module manufacturing, we have assumed $C_{inp}$ to be fractions of pF while the remaining $C_{tot}$ components to be about 1–2 pF. Clearly, particular values are strongly dependent on the chosen technology for the readout IC design and packaging as well as on the chosen connectivity scheme between CZT detector and the chip. It can be easily shown that the optimum peaking time $T_{opt}$ is given by the condition where $ENC_{th}$ is equal to $ENC_{dark}$ leading to the following expression:

$$
T_{opt}^2 = 4kT \frac{C_{tot}^2}{3g_mqI_{dark}}
$$

ENC is typically measured in the lab by measuring the output noise and referring it back to the input using the overall gain of the system. It is also possible to measure channel performance using the scope. By acquiring the channel shaper output signal on the oscilloscope at 1 MHz sampling frequency (e.g.,
5 msec observed time on 5,000 points), a Fast Fourier Transform (FFT) can be applied to the acquired data and the resulting spectrum calculated for each frequency. The noise expressed in mV is calculated as the standard deviation with respect to the shaper output average value and expressed as the equivalent noise in terms of electrons (by considering the known nominal gain of the data channel, typically about in the order of hundreds of mV per fC of the input charge). The result of these calculations is ENC value expressed in number of electrons, typically in a hundreds of electrons range depending what electronics is used, how high the count rate is, and the loading capacitance at the detector input.

3.2.5.4 Signal Shaping

The low-noise amplifier is typically followed by a filter, frequently referred to as the shaper, responding to an event with a pulse of defined shape and finite duration (width) that depends on the time constants and number of poles in the transfer function. The shaper’s purpose is twofold: first, it limits the bandwidth to maximize the signal-to-noise ratio; second, it restricts the pulse width in view of processing the next event. Extensive calculations have been made to optimize the shape, which depends on the spectral densities of the noise and system constraints (e.g., available power and count rate).

Optimal shapers are difficult to realize, but they can be approximated, with results within a few percent from the optimal, either with analog- or digital-processors, the latter requiring analog-to-digital conversion of the charge amplifier signal (anti-aliasing filter may be needed). In the analog domain, the shaper can be realized using time-variant solutions that limit the pulse width by a switch-controlled return to baseline or via time-invariant solutions that restrict the pulse width using a suitable configuration of poles. The latter solution is discussed here as it minimizes digital activity in the front-end channels.

In a front-end channel, the time-invariant shaper responds to an event with an analog pulse, the peak amplitude of which is proportional to the event charge, $Q$. The pulse width, or its time to return to baseline after the peak, depends on the bandwidth (i.e., the time constants) and the configuration of poles. The most popular unipolar time-invariant shapers are realized either using several coincident real poles or with a specific combination of real and complex-conjugate poles. The number of poles, $n$, defines the order of the shaper. Designers sometimes prefer to adopt bipolar shapers, attained by applying a differentiation to the unipolar shapers (the order of the shaper now is $n - 1$). Bipolar shapers can be advantageous for high-rate applications but at expenses of a worse signal-to-noise ratio.

In typical readout system, the shaping time varies from fraction of $\mu$s up to several $\mu$s. The shaping time is defined as the time-equivalent of the standard deviation of the Gaussian output pulse. In the laboratory, it is the full width of the pulse at half of its maximum value (FWHM) that is typically
being measured. FWHM value is greater than the shaping time by a factor of 2.35.

The DC component of the shaper from which the signal pulse departs is referred to as the output baseline. Since most extractors process the pulses’ absolute amplitude, which reflects the superposition of the baseline and the signal, it is important to properly reference and stabilize the output baseline. Non-stabilized baselines may fluctuate for several reasons, like changes in temperature, pixel leakage current, power supply, low-frequency noise, and the instantaneous rate of the events. Non-referenced baselines also can severely limit the dynamic and/or the linearity of the front-end electronics, as in high-gain shapers where the output baseline could settle close to one of the two rails, depending on the offsets in the first stages. In multiple front-end channels sharing the same discrimination levels, the dispersion in the output baselines can limit the efficiency of some channels.

### 3.2.5.5 Peak Detection

Peak detector is one of the critical blocks in the radiation signal detection system as accurate photon energy is determined by the detected peak amplitude. Standard PDs may be sampled or asynchronous solutions. Sampled PDs are more precise but suffer from high-circuit complexity and high-power dissipation. Asynchronous PDs have simpler structure but suffer from lower output precision.

### 3.3 Examples of XRD Readout ICs

There are literally hundreds of readout ICs that have been published in the literature. This section summarizes the design and performance characteristics of three photon counting and three spectroscopic devices.

#### 3.3.1 Photon Counting ICs

Fast readout electronic circuits have been developed to reach count rates of several millions counts per second [4–22]. These systems provide coarse energy resolution given by a limited number of discriminators and counters. This section provides some information about the most important photon-counting devices.

##### 3.3.1.1 TIMEPIX and MEDIPIX

MEDIPIX family consists of the several ICs grouped in two families: TIMEPIX and MEDIPIX. TIMEPIX readout IC is the ASIC developed in the framework
of the MEDIPIX2 collaboration [25]. The pixel matrix consists of $256 \times 256$ pixels with a pitch of $55 \mu m$ which gives a sensitive area of about $14 \times 14 \text{mm}^2$. TIMEPIX is designed in a $0.25 \mu m$ CMOS process and has about 500 transistors per pixel. The chip has one threshold and can be operated in photon counting (PC), time over threshold (ToT), or time of arrival (ToA) modes. The principles of the different operating modes are described in detail in the literature [25].

In the photon-counting mode, the counter is incremented once for each pulse that is over the threshold, while for the ToT mode the counter is incremented as long as the pulse is over the threshold. In the time of arrival mode, the pixel starts to count when the signal crosses the threshold and keeps counting until the shutter is closed.

While TIMEPIX is a general purpose chip, the MEDIPIX is aimed specifically at X-ray imaging [25]. It can be configured with up to eight thresholds per pixel and features analog charge summing over dynamically allocated $2 \times 2$ pixel clusters. The intrinsic pixel pitch of the ASIC is $55 \mu m$ as in TIMEPIX. Silicon die can be bump bonded at this pitch (fine pitch mode) and the chip can be run with either four thresholds per pixel in single pixel mode (SPM) or with two thresholds per pixel in charge summing mode (CSM). Optionally, the chip can be bump bonded with a $110 \mu m$ pitch, combining counters and thresholds from four pixels. Operation is possible in SPM with eight thresholds per pixel or in CSM having four thresholds and summing charge of a $220 \times 220 \mu m^2$ area.

Being a very versatile and configurable chip, there is also the possibility to utilize two counters per pixel and run in continuous read/write mode where one counter counts while the other one is being read out. This eliminates the readout dead time but comes at a cost of losing one threshold since both counters need to be used for the same threshold. Finally, the charge-summing mode is a very important feature to combat contrast degradation by charge sharing in semiconductors detectors with small pixels.

### 3.3.1.2 ChromAIX IC

Multi-energy resolving ASIC called ChromAIX has been designed by Philips Corporation to support Spectral CT applications. In order to enable K-edge imaging, at least three spectrally distinct measurements are necessary; for a photon-counting detector the simplest choice is to have at least the same number of different energy windows. With more energy windows, the spectrum of incident X-ray photons is sampled more accurately, thus improving the separation capabilities.

The ChromAIX ASIC accommodates a sufficient number of discriminators to enable K-edge imaging applications. Post-processing allows separating the Photo effect, Compton effect, and one or possibly two contrast agents with their corresponding quantification. The ChromAIX ASIC is a pixelated integrated circuit that has been devised for direct flip-chip connection to a direct
converting crystal like CZT. The design target in terms of observed count rate performance is 10 Mcps/pixel, which corresponds to approximately 27.2 MHz/pixel periodic pulses, assuming a paralyzable dead-time model. Although the pixel area in CT is typically about 1 mm², both the ASIC and direct converter feature a significantly smaller pixel or sub-pixel. In this way, significantly higher rates can be achieved at an equivalent CT pixel size, while further improving the spectral response of the detector via exploiting the so-called small-pixel effect. The sub-pixel should not be made too small, since charge-sharing effects then start to degrade the spectral performance. Very small pixels would need counter-measures as implemented in Medipix-3, the effectiveness of which at higher rates remains doubtful due to charge-sharing effects.

The ChromAIX ASIC consists of a CSA and a pulse shaper stage, as any other photon-counting device. The CSA integrates the fast transient current pulses generated by the direct converter, providing a voltage step-like function with a long exponential decay time. The shaper stage represents a band-pass filter that transforms the aforementioned step-like function into voltage pulses of a defined height. The height of such pulses is directly proportional to the charge of the incoming X-ray photon. A number of discriminator stages are then used to compare a predefined value (i.e. energy threshold) with the height of the produced pulse. When the amplitude of the pulse exceeds the threshold of any given discriminator, the associated counter will increment its value by one count.

In order to achieve 10 Mcps observed Poisson rates, which would typically correspond to incoming rates exceeding 27 Mcps, a very high bandwidth is required. The two-stage approach using a CSA and a shaper allows achieving such high rates while relaxing the specification of its components. The design specification in terms of ENC was 400 e-, which corresponds to approximately 4.7 keV FWHM. Simulations of the analogue front-end have been carried out to evaluate the noise performance of the channel. According to these simulations, the complete analogue front-end electronic noise (CSA, shaper, and discriminator input stage) amounts to approximately 2.51 mV_{RMS}, which in terms of energy resolution corresponds to approximately 4.0 keV FWHM for a given input equivalent capacitance.

### 3.3.1.3 PILATUS IC

PILATUS is a hybrid pixel detector system operating in the single-photon counting mode; it was developed at the Paul Scherrer Institut for the needs of macromolecular crystallography at the Swiss Light Source (SLS). A calibrated PILATUS module has been extensively characterized with monochromatic synchrotron radiation. The detector was also tested in surface diffraction experiments at the SLS, whereby its performance regarding fluorescence suppression and saturation tolerance were evaluated, and have shown to greatly improve the sensitivity, reliability, and speed of surface diffraction data acquisition.
The operation of the PILATUS ASIC is as follows. The incident photons are directly transformed into electric charge in the semiconductor sensor, which is transferred via the bump bond to the input of the readout pixel. A schematic of the PILATUS readout chip pixel cell is presented in Figure 3.8. The analog front-end of a readout pixel consists of a charge-sensitive pre-amplifier (CSA) and an AC coupled shaper. The gain and shaping time of the CSA are adjusted with a global voltage ($V_{rf}$). An analog pulse from the shaper is discriminated against a threshold in the comparator after amplification. The comparator threshold of each pixel is set with a global threshold voltage ($V_{cmp}$) and is further individually trimmed using an additional in-pixel 6-bit digital-to-analog converter (DAC). If the pulse amplitude exceeds the threshold, a digital signal is produced which increments the 20-bit counter. This detection principle is free of dark current and readout noise effects but requires precise calibration of the pixel threshold for optimum performance.

3.3.2 Spectroscopic ICs

3.3.2.1 IDEF-X

IDef-X HD is the last generation of low-noise radiation-hard front-end ASICs designed by CEA/Leti for spectroscopy with CZT detectors [23]–[24]. The chip, as shown in Figure 3.9, includes 32 analog channels to convert the impinging charge into an amplified pulse shaped signal and a common part for slow control and readout communication with a controller.

![Architecture of the PILATUS IC readout cell](image-url)
The first stage of the analog channel is a charge-sensitive preamplifier (CSA) based on a folded cascode topology with an inverter input amplifier. It integrates the incoming charge on a feedback capacitor and converts it into voltage; the feedback capacitor is discharged by a continuous reset system realized with a PMOS transistor. The increase of drain current in this transistor during the reset phase is responsible for a non-stationary noise; to reduce the impact of this noise on the equivalent noise charge, a so-called non-stationary noise suppressor was implemented for the first time in this chip version using a low-pass filter between the CSA output and the source of the reset transistor to delay this noise.

The second stage is a variable gain stage to select the input dynamic range from 10 fC (250 keV) to 40 fC (1 MeV). The third stage is a pole zero cancellation (PZ) implemented to avoid long-duration undershoots at the output and to perform a first integration. The next stage of the analog channel is a second-order low-pass filter (RC\(^2\)) with variable shaping time. To minimize the influence of the leakage current on the signal baseline, a so-called baseline holder (BLH) was implemented by inserting a low-pass filter in the feedback loop between the output of the RC\(^2\) filter and the input of the PZ stage. The DC level at the output is stabilized for leakage current up to 7 nA per channel. The output of each analog channel feeds a discriminator and a stretcher. The discriminator compares the amplitude with an in-pixel reference low-level threshold to detect events. The stretcher consists of a PD and

FIGURE 3.9
32-channel IDEF-X IC architecture.
a storage capacitor to sample and hold the amplitude of the signal which is proportional to the integrated charge and hence to the incident energy. In addition, each channel can be switched off by slow control programming to reduce the total power consumption of the ASIC when using only few channels of the whole chip.

The slow control interface was designed to minimize the number of signals and to get the possibility to connect together up to 8 ASICs and address them individually. This optimization has allowed reducing the electrical interface from 49 pins in Caliste 256 to 16 pins in Caliste-HD for the same number of channels using low-voltage differential signals (LVDS). When an event is detected by at least one channel, a global trigger signal (TRIG) is sent out of the chip. The controller starts a readout communication with 3 digital signals (DIN, STROBE, and DOUT) to get the address of the hit ASIC and then the hit channels. Then the amplitudes stored in the peak detectors of the hit channels are multiplexed and output using a differential output buffer (AOUT). The whole readout sequence lasts between 5 and 20 μs, according to the set delays and clock frequencies and the number of channels to read out.

### 3.3.2.2 VAS UM/TAT4

The VAS UM/TAT4 ASIC chip is used to read-out both the amplitude of charge induction and the electron drift time independently for each anode pixel [27]. This readout IC has 128 channels, each with a charge-sensitive preamp and two CR–RC unipolar shapers with different shaping times. The slow shaper has 1-μs peaking time and is coupled to a peak-hold stage to record pulse amplitude. The fast shaper has a 100-ns shaping time and is coupled to simple level discriminators for timing extraction.

Of the 128 channels, 121 are connected to the pixels, 1 is connected to the grid, and 1 is connected to the cathode. Compared to the anodes, the polarity of the signals is reversed for the cathode and grid. The peak-hold properties, signal shaping, ASIC noise, and triggering procedures are included in the ASIC read-out system model. The fast shaper can trigger off pulses as small as 30 keV for the anode and 50 keV for the cathode. Only the pixels with slow-shaped signals greater than a noise discrimination threshold of 25 keV are used in operation.

VAS UM/TAT4 is particularly well suited for three-dimensional imaging and detection using thick CZT detectors (>10 mm) with high-energy photons (>1 MeV). Three-dimensional position-sensing techniques enable multiple-pixel events of pixelated CZT detectors to be used for 4π Compton imaging. Multiple-pixel events occur by either multiple gamma-ray interactions or charge sharing from a single electron cloud between adjacent pixels. To perform successful Compton imaging, one has to correct for charge sharing. There is a large research effort at University of Michigan under direction of Professor Zhong He to resolve these complicated signal processing issues and to re-construct the trajectory of incoming photons for dirty bomb
detection and other high-energy applications that might or might not be relevant to the XRD imaging.

### 3.3.2.3 HEXITEC

HEXITEC was a collaborative project between the Universities of Manchester, Durham, Surrey, Birkbeck, and The Science and Technology Facilities Council (STFC) Technology Facilities Council (STFC). The objective of the program was to develop a new range of detectors such as CZT for high-energy X-ray imaging applications. The project has been funded by EPSRC on behalf of RCUK under the Basic Technology Program.

The HEXITEC ASIC consists of a $80 \times 80$ pixel array on a pitch of 0.25 mm [26]. Each pixel contains a 52 $\mu$m bond pad which can be gold stud bonded to a CZT detector. Figure 3.10 shows a block diagram of the electronics contained in each HEXITEC ASIC pixel. Charge is read from each of the CZT detector pixels using a charge amplifier, which has a selectable range and a feedback circuit which compensates for detector leakage currents up to 50 pA.

The output from each charge amplifier is filtered by a 2 $\mu$s peaking circuit comprising a CR–RC shaper followed by a second-order low-pass filter. A peak hold circuit maintains the voltage at peak of the shaped signal until it can be read out. Three track-and-hold buffers are used to sample the shaper and peak hold voltages sequentially prior to the pixel being read.

![FIGURE 3.10](image)

**FIGURE 3.10**

Block diagram of the HEXITEC architecture.
The HEXITEC is read out using a rolling shutter technique. A row select register is used to select the row which is to be read out. The data from each pixel becomes available on all column outputs at the same time, and at this point, the peak hold circuits in that row can be reset to accept new data. The data being held on the column output is read out through a column multiplexer. The column readout rate is up to 25 MHz and the total frame rate depends on the number of pixels being read out. The main limitation of the HEXITEC is a maximum count rate due to 10 kHz frame readout scheme.

3.4 Readout IC Operational Issues

3.4.1 Threshold Equalization

As part of the pixel detector calibration, the ASIC chip has to be equalized in order to minimize the threshold dispersion between pixels. This requirement results from the fact that the threshold that the pixel sees is applied globally but the offset level of the pixel can be slightly different due to process variations affecting the baseline of the preamplifier.

The equalization is performed with a threshold adjustment DAC in each pixel. The resolution of the adjustment DAC is usually in the range of 4 bits depending on particular ASIC implementation. The standard way to calculate the adjustment setting for each pixel is by scanning the threshold and finding the edge of the noise, then aligning the noise edges. This adjusts correctly for the offset level of the pixel but gain variations can still deteriorate the energy resolution at a given energy. To correct for the gain mismatch, either test pulses or monochromatic X-ray radiation has to be used for the equalization. Equalizing at the energy of interest instead of the zero level might be also preferred.

3.4.2 Energy Calibration

Depending on the ASIC architecture, there are two types of energy calibration that needs to be done: calibration of the threshold and calibration of the time over threshold response (if applicable). For photon-counting chips as MEDIPIX, the only calibration required is the threshold response while in time over threshold readout ICs such as TIMEPIX the ToT response has to be calibrated as well. Virtually all spectroscopic ICs need to undergo energy calibration procedures as electronics circuitry basically has no understanding of photon energy expressed in keV.

To calibrate the threshold, we need monochromatic photons or at least radiation with a pronounced peak. These can be obtained from radioactive sources, by X-ray fluorescence, or from synchrotron radiation like Am241 and/or Co57 point sources. To find the corresponding energy for a certain
threshold, the threshold is scanned over the range of the peak obtaining an integrated spectrum. The data is then either directly fitted with an error or sigmoid function or first differentiated and then fitted with a Gaussian function. From this fit, the peak position and energy resolution can be extracted. Repeating the procedure for multiple peaks the result can then be fitted with a linear function, and the relationship between voltage threshold setting and deposited energy in the detector is found.

3.4.3 Charge Sharing Corrections

Charge sharing between pixel is a highly detrimental effect in XRD signal detection as explained in Chapter 2. To illustrate the techniques used for charge sharing correction, it is helpful to review charge sharing using the diagrams shown in Figure 3.11.

Suppose that a pixelated detector is divided into 9 pixels as shown in Figure 3.11a. If a X-ray photon strikes pixel 5 near the center as in Figure 3.11b, then most of the charge will be localized to that pixel and very little charge sharing will occur. However, if the photon lands near the pixel boundaries as in Figure 3.11c, then the charge will be shared amongst pixels 1, 2, 4, and 5; low energy events will be detected in the pixels 1, 2, and 4, creating a low energy tail in the spectrum. To correctly detect the energies of the incoming photons, the system must recognize that a single photon event has spread its charge in a cluster of pixels, determine where the photon has most likely landed (usually the pixel with the largest charge deposition), and assign all surrounding charge to that single pixel.

In general, when the pixel size is starting to approach the size of the charge cloud, the input signal is subjected to charge sharing. Charge sharing creates a characteristic low energy tail and leads to a reduced contrast and distorted spectral information. To counteract this problem, there are two possibilities, either to use larger pixels (reduced spatial resolution) or to implement charge summing on a photon by photon basis.

For lower rates and with detectors that store the energy information in each pixel either using ToT (TIMEPIX) or a peak-and-hold circuit (HEXITEC), the

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**FIGURE 3.11**
Charge sharing in a pixelated detector.
charge summing can be done offline. However, this requires that you do not have a second hit in the same pixel before you read the first one out. Using this approach, you also lose charge that is below the detection threshold.

With a photon near the pixel boundaries as in Figure 3.12a, most of the charge is collected by the center pixel and some of the charge is shared with adjacent pixels. Some readout ICs are able to recognize that these events are coincident in time and reassign the charge to the correct pixel. The MEDIPIX readout IC from CERN was the first ASIC to implement this algorithm called the Charge Summing Mode (CSM), where the analog charge can be summed up in a $2 \times 2$ cluster before being compared to the threshold. MEDIPIX IC also has a mode in which this functionality is disabled, called the Single Pixel Mode (SPM).

The advantage of this approach is that it can handle much higher interaction rates and that even charge below the threshold is summed as long as one pixel is triggered. However, since this correction has to be implemented in the ASIC architecture, it complicates the chip design and is less flexible when interfacing with various interconnects.

### 3.4.4 Pile-Up Effects

Given that the processing of each photon takes time, there will be problems with pileup effects at high count rates. Pileup happens when a second photon arrives in the same pixel before the first one is processed. Depending on the system architecture, the second photon could either be lost or added to the signal of the first photon. The result will be a deviation from linear behavior for the count rate. This deviation can be corrected for up to a certain limit in photon-counting devices, but more problematic are the spectral distortions due to pileup that cannot be corrected for. For this reason, the operation of spectroscopic ASIC is limited to the maximum count rate that is not causing any pileup effects. Different detectors will have different responses and it is important that the detector is characterized and is suitable for the flux in a specific application. Since the flux is measured per area, smaller pixels offer an advantage of a smaller number of photons per second per pixel.

![FIGURE 3.12](a) Charge sharing correction in a pixelated detector.
The X-ray photon events in the CZT detector occur randomly following a Poisson distribution. The probability density function between successive events is given by [5]:

\[ p(t) = r \cdot \exp(-rt) \]

where \( r \) is the average incoming photon rate. While pile-up occurs, there will be a deviation from the linear relationship between flux rate and count rate; as illustrated by the PILATUS curves shown in Figure 3.13, the count rate in the ASIC begins to saturate as the flux rate increases beyond a certain limit.

An equivalent way of characterizing this limitation is via a parameter called dead time, which is the minimum amount of time that must separate photon arrivals for them to be counted separately. If successive photons arrive within this dead time window, paralysis occurs in the readout IC count as shown in Figure 3.14.

As illustrated in Figure 3.14, a single photon generates a pulse which is counted correctly. Subsequently, two photons arrive within the dead time window and is only counted as one event. Finally, multiple photons arrival causes pulse overlaps such that the pulse shaper output does not fall below the threshold and paralysis occurs in the IC count.

Modern ICs combat this problem by introducing non-paralyzable counting modes. An example of the implementation is the PILATUS3 Instant Retrigger Architecture. This is accomplished by re-evaluating the pulse shaper output after a programmable amount of time. If the output is still above threshold, it is assumed that pileup has occurred and the counting circuit is retriggered. This technique prevents the count rate from freezing due to multiple photon arrivals.

![FIGURE 3.13](image.png)

**FIGURE 3.13**
PILATUS3 ASIC count rate vs. incoming flux rate [33].
3.4.5 Dark Current Correction

Even when no photons strike the detector, each pixel can still produce some charge due to leakage currents from the detector and the ASIC itself. Hence a calibration procedure is performed at start-up called dark current correction. With no X-ray source and the detector in the “dark,” the value of each pixel is read and stored into memory. When the system is running, this dark current value is subtracted from the raw value of each pixel, hence removing the artifacts due to the leakage currents. It is also possible to correct for dark current contribution by re-designing analog front-end so the correction happens simultaneously with the photon detection.

An example of one of the dark current schemes is shown in Figure 3.15. After dark current correction, each pixel is compared to a programmable threshold to determine whether a valid event has occurred. This process is
used to further remove any noise from the data. A pixel value that is above the threshold is called a valid event for the discussion below.

3.5 Conclusions

Currently, most digital radiation detectors for security applications are based on integrating the X-ray quanta (photons) emitted from the X-ray tube for each frame. This technique is vulnerable to noise due to variations in the magnitude of the electric charge generated per X-ray photon. Higher energy photons deposit more charge in the detector than lower energy photons so that in a quantum integrating detector, the higher energy photons receive greater weight. This effect is undesirable in many detection applications because the higher part of the energy spectrum provides lower differential attenuation between materials, and hence, these energies yield images of low contrast.

Direct conversion X-ray quantum counting detectors solve the noise problem associated with photon weighting by providing better weighting of information from X-ray quanta with different energies. In an X-ray quantum counting system, all photons detected with energies above a certain predetermined threshold are assigned the same weight. Adding the energy windowing capability to the system (i.e., counting photons within a specified energy range) theoretically eliminates the noise associated with photon weighting and decreases the required X-ray dosage by up to 40% compared to integrating systems.

Direct conversion detectors are also essential to XRD detection and imaging applications where precise information about the energy of incoming photons is crucial. This chapter reviews key challenges that are present in spectroscopic and photon-counting electronics for XRD. Energy resolution, charge-sharing correction, high flux capability, and pileup effects affect both the count rate linearity and the spectral response. One way to counteract that problem is to use smaller pixels, but smaller pixel will lead to more charge sharing. In this respect, the various chips offer an interesting combination of relatively small pixels and still very good energy resolution.

The readout integrated circuits (ROIC) design issues have been discussed in detail in this chapter. A summary classification of those ICs is shown in Figure 3.16. The ROIC family can be divided into spectroscopy and photon-counting chips. The photon-counting chips usually operate in a synchronous manner while the spectroscopic chips can be both asynchronous and synchronous. Although over 100 ROIC have been designed and used, it is no doubt that new designs will enter the marketplace in the next 5–10 years and are likely to be based on very advanced CMOS chip fabrication technologies.
Integrated Circuits for XRD Imaging

References


